REMARKS

Applicant acknowledges the Advisory Action dated January 21, 2005. The Examiner is respectfully requested to reconsider the arguments provided in the response dated December 30, 2004 and to withdraw all claim rejections in view of those arguments and the following remarks provided in rebuttal to the Examiner's comments in the Advisory Action.

Regarding the Examiner's comments relative to part 1 of the applicant's response, the Examiner reforms paragraph 34 of the previous Office Action to state that the input period Tp is "delayed" by the number of N or M delay elements rather than "adjusted". However, such rewriting of the office action does not detract from applicant's point that the resolutions with which the first and second means of the applicant's apparatus of claim 1 adjust the path delay are integer fractions Tp/M and Tp/N of the period Tp of the pulse sequence being delayed. The total delay of HEYNE's circuit is of course a function of the number M and N of inverters I1 and I2 in the signal path, however, the number of inverters in the signal path and the total amount by which HEYNE's input signal is delayed says nothing about the resolution with which it can adjust path delay. As discussed in detail in the previous response, the resolution with which HEYNE's circuit can adjust signal delay is a function of the particular delay provided by each individual inverter I1, not the total number of inverters I1 and I2 that might currently be in the signal path, and not the total amount by which the input signal is delayed.

HEYNE's circuit can adjust delay by changing the number of inverters I1 in the path from M to M+1 or M-1, or by changing the number of inverters I2 in the path from N to N+1 or N-1. Thus, the resolution with which path delay can be adjusted (i.e. the smallest amount by which the path delay can be changed), which HEYNE teaches is the amount of delay of one inverter I1, which is an integer fraction of the delay of one inverter I2. (See col. 5, lines 49-55.) HEYNE does not teach or suggest that the delay of either I1 or I2 should have any relationship to the period Tp of the signal being delayed, and in particular does not teach that

they should be fixed functions Tp/N and Tp/M of the period Tp of the input signal as recited in claim 1. The fact that HEYNE's circuit delays the signal by M inverters I1 and N inverters I2 does not detract from applicant's argument regarding the recited delay resolutions of Tp/M and Tp/N.

Regarding the Examiner's comments relative to parts 2a-2c of the applicant's last response, it appears the Examiner now correctly concedes that HEYNE's schematic alone do not teach or suggest that the delays of inverters I1 and I2 are Tp/M and Tp/N, and that if HEYENE's schematic does teach or suggest such thing, then we must look elsewhere within HEYNE's specification for such teaching. Accordingly, the Examiner makes the following argument in support of the assertion that HEYNE's specification teaches this:

"[O]ne with ordinary skill in the art would have recognized that HEYNE's apparatus does advocate the delay resolutions to be integer fractions of the period of an input signal in order to have a practical apparatus that can incrementally adjust the delay circuits to achieve synchronization."

Thus, it appears the Examiner is of the opinion that HEYNE's circuit would be useless for the purposes intended unless the delays of inverters I1 and I2 were precise functions Tp/M and Tp/N of the period Tp of the input signal to HEYNE's circuit. The Examiner is respectfully requested to reconsider this opinion in view of the following arguments.

(1) One of skill in the art would understand that to be practical, HEYNE's circuit should be able to delay signals of more than one particular period Tp. HEYNE does not warn us that the circuit will work with an input signal having one and only one particular period. If, as the Examiner supposes, the delays of inverters I1 and I2 must be Tp/M and Tp/N in order for the circuit to be practical, then it would follow that the delays of inverters I1 and I2 must be adjusted in some way whenever the input signal period is changed. What adjusts the delays of

inverters I1 and I2 to accommodate changes in the period Tp? Nothing in any of HEYNE's drawings or specification shows, describes or suggests any mechanism for setting delays of inverters I1 and I2 as functions of Tp (Tp/M and Tp/M) regardless of the value of Tp. HEYNE does not explicitly indicate that we have to change the delays of inverters I1 and I2 when we change Tp. So how is it that one of skill in the art would assume that the delays of I1 and I2 are somehow functions of Tp?

(2) The mere fact that HEYNE says the delay of the delay is adjusted during an initialization process so that the output signal is "in phase" with the input signal does not necessarily imply to one of skill in the art anything about the particular resolution with which such a delay adjustment is made or, in particular, about the particular amount of delay each inverter I1 and I2 provides. If the input and output signals must be precisely in phase (as the Examiner appears to believe), then the sum of delays of the inverters in the signal path must precisely equal the period of the input signal, and that would of course imply, as the Examiner concludes, that I1 and I2 should have delays that are integer fractions of Tp. However, those of skill in the art will understand that it is not necessary to the practicality of HEYNE's circuit for delay to be adjusted to place the input and output signals precisely in phase. A skilled artisan would understand that HEYNE's delay circuit need only be adjusted so that its input and output signals are as nearly in phase with one another as is possible given the resolution with which the circuit delay can be adjusted, whatever that resolution may be. Nothing in HEYNE teaches that the phase adjustment must so precise that the inverter delays must be integer fractions of Tp, and as discussed below, such precision is not necessary for proper operation of HEYNE's circuit.

(3) Although the Examiner maintains that HEYNE's circuit would be impractical unless the delays of inverters I1 and I2 are precise functions Tp/N and Tp/M of the period of the signal being

delayed, the Examiner does not indicate why he is of this opinion. HEYNE's circuit is completely practical even though the delays of inverters I1 and I2 are not functions of Tp. The purpose of HEYNE's circuit is to delay a signal by some adjustable amount over a wide range, with a desired degree of resolution by providing an appropriate number of inverters I1 and I2 in the signal path. HEYNE points out that the circuit can be calibrated during an initialization procedure to provide a desired delay even though the delays of inverters I1 and I2 are functions of temperature. HEYNE points out that since the delays of inverters I1 and I2 are temperature dependent, it is not possible to predict the delay of the delay circuit from the number of inverters I1 and I2 placed in the signal path. HEYNE therefore teaches to calibrate the circuit for a desired delay by applying an input signal having a period Tp matching the desired delay. We select the number of inverters I2 to grossly adjust the delay and the number of inverters I1 to finely adjust the delay so that the circuit's input and output signals are "in phase". See HEYNE's abstract and also column 2, lines 4-47. This sets the delay to the period Tp of the input signal, with a resolution equal to the delay of one inverter I1. Thereafter the circuit will always delay any signal applied to it by that particular delay, provided, of course, it remains at the same temperature. (Of course, one failing of HEYNE's delay circuit not shared by the applicant's delay circuit is that if the circuit temperature changes, it is necessary to recalibrate the circuit.)

HEYNE's circuit is therefore completely practical for providing a delay that is adjustable with a resolution equal to the delay of one inverter I1 because that is the smallest amount by which we can adjust the delay provided by HEYNE's circuit. What should the delay of one inverter I1 be? HEYNE teaches only that the sum of delays of inverters I1 should equal the expected range of variation in delay due to temperature when all of inverters I2 are selected. Hence, if there are M inverters I1, then HEYNE's circuit can be calibrated to compensate for variations in temperature with a resolution 1/Mth the expected

range of temperature-dependent delay variation through inverters I2. Nothing in HEYNE teaches, mandates or even suggests that the delays of inverters I1 or I2 can or should be some integer fraction of the period of the circuit input signal. Such a notion is unnecessary to the stated function of HEYNE's delay circuit. HEYNE's circuit is completely practical and carries out the function it is intended to carry out (control delay with a resolution that is a fraction of the temperature variation range) even though the delays of inverters I1 and I2 are not functions of the period of its input signal.

(4) The notion that HEYNE's inverters might have delays that are functions of input signal period Tp rather than functions of temperature is inconsistent with much of the premise of HEYNE's teaching. Note that the delay provided by HEYNE's circuit varies with temperature and that, as HEYNE teaches, if we want to maintain some desired delay in the face of temperature variation, we have to experimentally adjust the number of inverters I1 in the path when temperature changes in order to maintain the delay at a desired setpoint. What is it in HEYNE's circuit that changes with temperature? Of course, it is the delays of inverters I1 and I2. This is the problem HEYNE's circuit addresses: given delay elements having delays that change with temperate, how do we provide a particular delay when the circuit is at some particular temperature? That is why HEYNE teaches us that we must size the nominal delay of the number of inverters I1 to be some desired fraction of the total expected variation in delay and then experimentally adjust the number of inverters I1 in the path to compensate for the actual temperate of the circuit.

Therefore, given that HEYNE teaches us that the delays of inverters I1 and I2 are temperature dependent, how is it that the Examiner concludes the one of skill in the art would conclude that inverters I1 and I2 must have delays that are precisely Tp/N and Tp/M? The Examiner's assumption implies that the delays of inverters I1 and I2 are <u>temperature independent,</u> exactly opposite of what HEYNE teaches. How can the delays have any fixed

relation to Tp when they vary with temperature? If they must be precisely Tp/N and Tp/M for HEYNE's circuit to be useful, then the delays of inverters I1 and I2 would not vary with temperature and there would be no need, as HEYNE teaches, to experimentally adjust the number of inverters I1 during initialization to compensate for temperature variation. We would know what the delays are simply by knowing how many of each inverter I1 and I2 is in the signal paths.

This is an advantage of the applicant's circuit not shared by HEYNE's circuit. Note that the delays of the applicant's delay elements are completely independent of the temperature of the delay circuit. Their delay is precisely determined by the period of the input signal, and as long as the input signal has a period that is independent of temperature, the applicant's circuit will provide the same delay. It matters not whether the applicant's circuit lies in the snow at the North Pole or fries under the sun in the Sahara, there is no need to adjust the number of elements in the signal path to compensate for variation in delay due to temperature variation. That is why the applicant's invention is concerned with a delay circuit having first and second means with delay resolutions that are functions of the input signal period Tp rather than functions of temperature as taught by HEYNE. The applicant's circuit solves the problem of temperature variation in delay elements by using elements having delays that are functions of Tp and that do not vary with temperature. Hence, there is no need for the kind of compensation HEYNE teaches.

(5) HEYNE teach that the resolution of a delay circuit formed by a variable number of delay elements is equal to the unit delay of one inverter I1. That is why HEYNE teaches to finely adjust delay only by adjusting the number of inverters I1. If we want to adapt HEYNE's circuit for higher resolution, it would be obvious to provide more inverters I1 having smaller delays. However, there is a limit to how fast an inverter can switch and therefore a limit to how small a delay it can provide. The applicant's invention solves that problem by providing two

delay circuits ("first and second means") in series wherein one delay circuit has a delay resolution of Tp/N and the other a delay resolution of Tp/M as recited in claim 1, and by making N and M relatively prime as recited, for example in claim 2. In doing so, the applicant provides a delay circuit that (quite surprisingly) has a delay adjustable with a resolution that is much higher than either Tp/N or Tp/M. The resolution of the applicant's circuit is therefore smaller than the delay of any single delay element in the circuit.

Regarding the Examiner's comments to part 3 of applicant's reply to the Final Office Action, the Examiner has not contradicted the applicant's assertion that FIG. 3 of HEYNE does not tell us anything about the period of the input signal of HEYNE relative to the values of t1 and t2. Further, the example cited by the Examiner (N=1 and M=4) does not meet the terms of claim 1, 20 or 34, each of which requires that both M and N be greater than one, and does not meet the requirement of claims 2, 5, 21, 24, or 34 that M and N be relatively prime.

Regarding part 4 of the applicant's reply, the Examiner correctly observes that HEYNE teaches that the number of second delay elements is incremented during initialization so that the desired phase of the output signal is "close enough" to the desired phase and then held constant, and the number of first delay elements is then adjusted to compensate variation in delay due to temperature variation. As discussed above, if HEYNE teaches that the delays of the first and second elements are integer fractions of the period of the input signal rather than functions of the period of the input signal, it would not be necessary to adjust the number of first inverters to compensate for temperature variations since there would be no such temperature variations.

The Examiner is none the less of the opinion that HEYNE teaches the sum of delays of inverters I1 is Tp, and given that

(incorrect) assumption, the Examiner maintains that FIG. 3 teaches that

$$12*t1 = Tp$$

and

$$K*t2 = (5/3)Tp$$

where

t1 is unit delay of each inverter I1,
t2 is unit delay of each inverter I2 and
K is total number of elements I2.

This implies that

$$t1 = (3K/60)t2$$

Looking at FIG. 3, we see

$$t1 = t2/4$$

which implies K is 5.

If K is 5 then, given the Examiner's assumption that 12*t1=Tp,

$$t1 = Tp/12$$
$$t2 = Tp/3$$

This implies M = 12 and N = 3, which are not relatively prime as recited in claim 2.

In any case the Examiner's assumption that HEYNE's FIG. 3 or any other part of HEYNE teaches that the sum of delays of elements I1 or the sum of delays of elements I2 are functions of Tp is incorrect for the reasons discussed above. HEYNE clearly

teaches that the delays of these elements are functions of temperature, which is inconsistent with the Examiner's conclusion that they are fixed functions Tp/M and Tp/N of input signal period. FIG. 3 provides no information about Tp and no part of HEYNE's discussion of FIG. 3 says or implies anything about any fixed relationship between delays of inverters I1 and I2 and the period Tp of the signal used to calibrate the circuit.

The Examiner is of the opinion that the applicant cannot attack references individually when rejections are based on combinations of references. It is true that when a rejection cites two references A and B, the applicant cannot rely on an argument that neither A nor B discloses the invention. However the applicant's response to the Final Office Action did not err in this manner. When a claim recites elements X and Y, and the Examiner cites reference A for showing element X but not Y, and cites reference B as showing element Y but not X, then the applicant may defeat the rejection by any one of the following:

1. showing reference A fails to teach element X
2. showing reference B fails to teach element Y.
3. showing that it would not be obvious to combine the two references.

In the rejection of claim 1, the Examiner cites HEYNE (reference A) but not HONDEGHEM (reference B) as teaching the recited first and second means having delay resolutions of Tp/N and Tp/M (element X). Hence, the applicant's remarks of pages 1 6 of the last response correctly attack HEYNE as failing to teach the first and second means, for it is on HEYNE the Examiner relies for disclosing these elements.

The Examiner cites HONDEGHEM as disclosing the programmable sequencer recited in claim 1 (element Y) and correctly concedes HEYNE does not. Hence, the applicant's comments of pages 7-9 correctly attack HONDEGHEM as failing to disclose the recited

programmable sequencer, for it is on HONDEGHEM the Examiner relies as disclosing that element.

The applicant's arguments of pages 7-9 also address the combination of HEYNE and HONDEGHEM by showing that while HONDEGHEM (col. 6, lines 30) describes FIG. 3 as showing a repetitive waveform, the waveform has nothing to do with controlling delay circuits of the type disclosed by HEYNE, and therefore it would not be obvious to one of skill in the art to use such repetitive waveforms as control inputs to HEYNE's circuits. The applicant's previous arguments point out that the cited section of HONDEGHEM clearly teaches that the repetitive waveform drives a D/A converter 163 (Fig 2), and does not teach that the repetitive waveform controls any kind of delay circuit. See the last paragraph of page 8 and the top of page 9 of the applicant's response. The fact that a reference shows a repetitive waveform does not render obvious every possible use of a repetitive waveform. The references should motivate one skilled in the art to use the waveform in the context claimed. HONDEGHEM motivates one only to apply a repetitive waveform to a D/A converter. Thus, the applicant's augments against the rejection of the claims over the combination of HEYNE and HONDEGHEM are correct in both form and substance and the Examiner has failed to adequately rebut those arguments.

Regarding the rejections of claims in view of the combination of HEYNE, HONDEGHEM and LIEDBERG, the Examiner cites HEYNE and HONDEGHEM as teaching the subject matter of claim 8, but not the additional limitations of claim 9, and cites LIEDBERG as teaching the additional subject matter of claim 9 but not the subject matter of parent claim 8. The applicant's last response therefore correctly attacked HEYNE and HONDEGHEM as failing to teach the subject matter of claim 8 and attacked LIEDBERG as failing to teach the additional elements of claim 9. Note that the Examiner has conceded at section 23 of the final office action that HEYNE and HONDEGHEM fail to teach the additional subject matter of claim 9. Thus, it is necessary for the

applicant at pages 10 and 11 of the last response to attack only LIEDBERG as failing to teach the additional subject matter.

In view of the foregoing remarks, it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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